(12) UK Patent Application (19) GB (11) 2 218 816(13)A

(43) Date of A publication 22.11.1989

(21) Application No 8811863.3

(22) Date of filing 19.05.1988

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(51) INT CL⁴
G01R 31/28

(52) UK CL (Edition J)
G1U UC9C
U1S S2088

(56) Documents cited
None

(58) Field of search
UK CL (Edition J) G1U, G4A
INT CL⁴ G01R, G06F

(54) Testing integrated circuits

(57) An integrated circuit with self-test facility comprises combinational logic blocks (Ce-Cn) interleaved test registers (R1-R8) the latter each comprising (Fig 4) at least two test registers providing at least a two stage delay whereby one state holds test patterns whilst the other holds compressed test results. The logic blocks (Ce-Ch) are driven by a common input interleaved test register (R1) and by respective input interleaved test registers (R1-R4), the output of each block being coupled to respective output interleaved test registers (R5-R8). A scan path through the common interleaved test register diverges into a plurality of scan paths (102, 104, 106) through the registers, the scan paths reconverging at a logic function (98) for modulo-2 addition on the incoming data whereby there is conservation of all of the analysed information including any originally presented to the common interleaved test register.

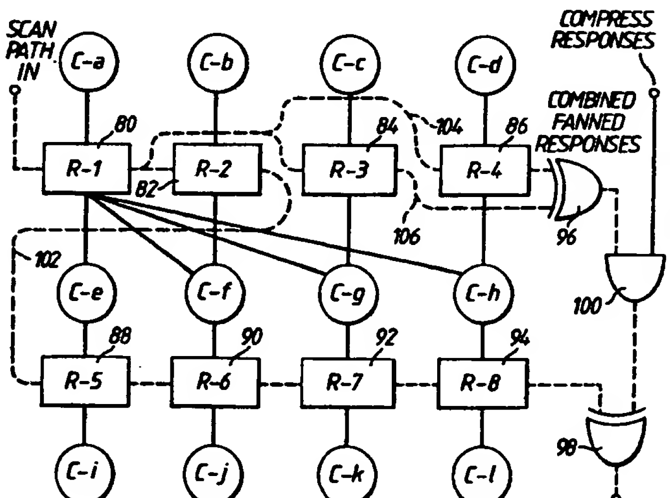


Fig.2(B).

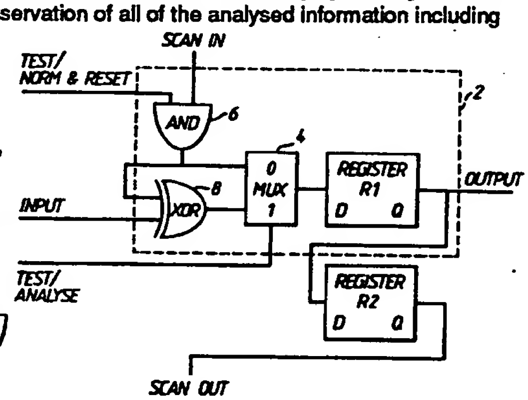


Fig.4.

GB 2 218 816 A

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

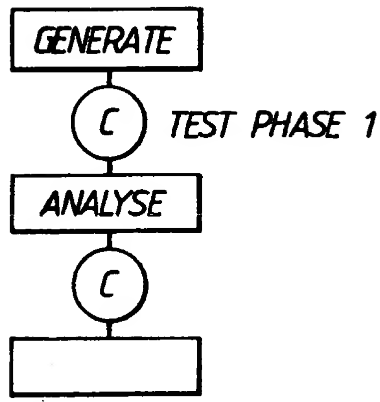


Fig.1(A).
PRIOR ART

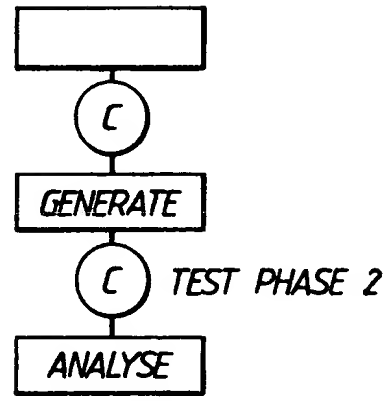


Fig.1(B).
PRIOR ART

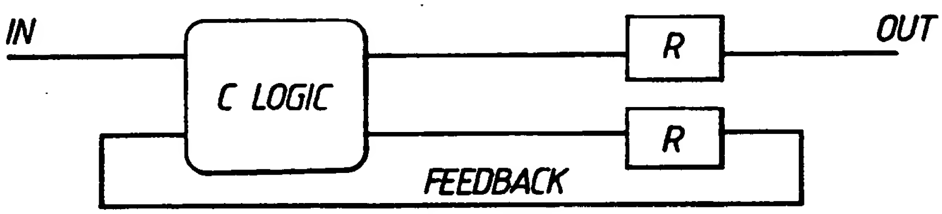


Fig.1(C).
PRIOR ART

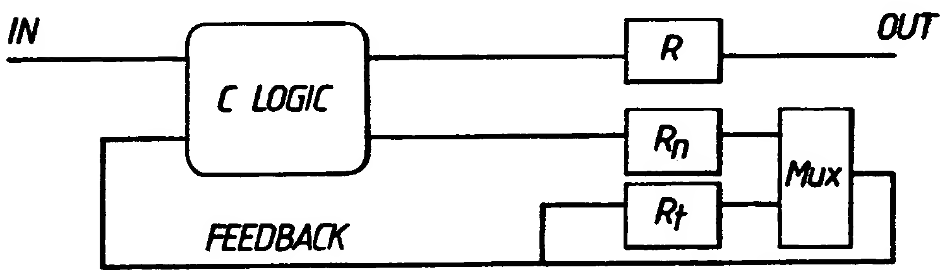


Fig.1(D).
PRIOR ART

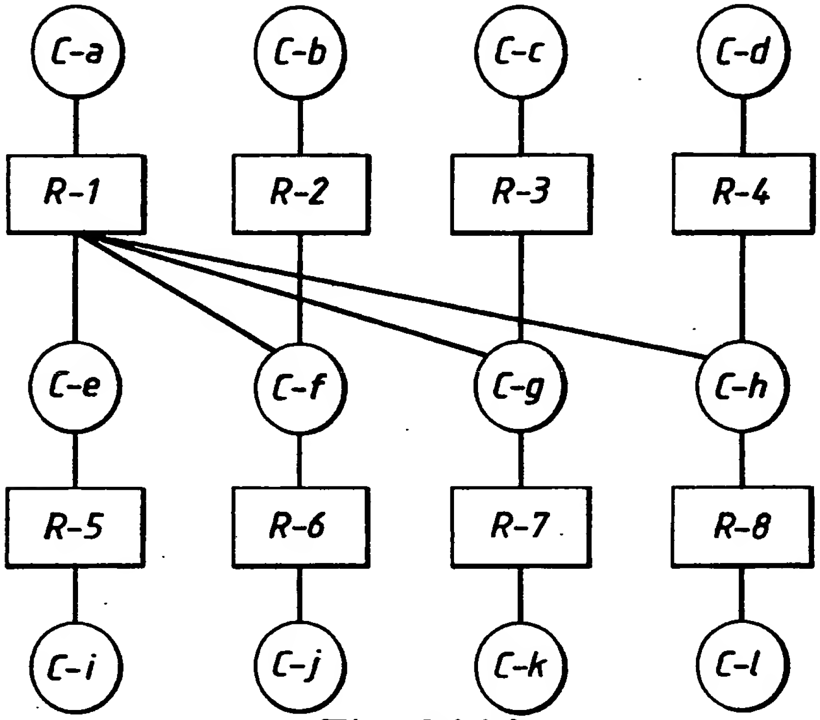

C-a
C-b
C-c
C-d
R-1
R-2
R-3
R-4
C-e
C-f
C-g
C-h
R-5
R-6
R-7
R-8
C-i
C-j
C-k
C-l

Fig.2(A).

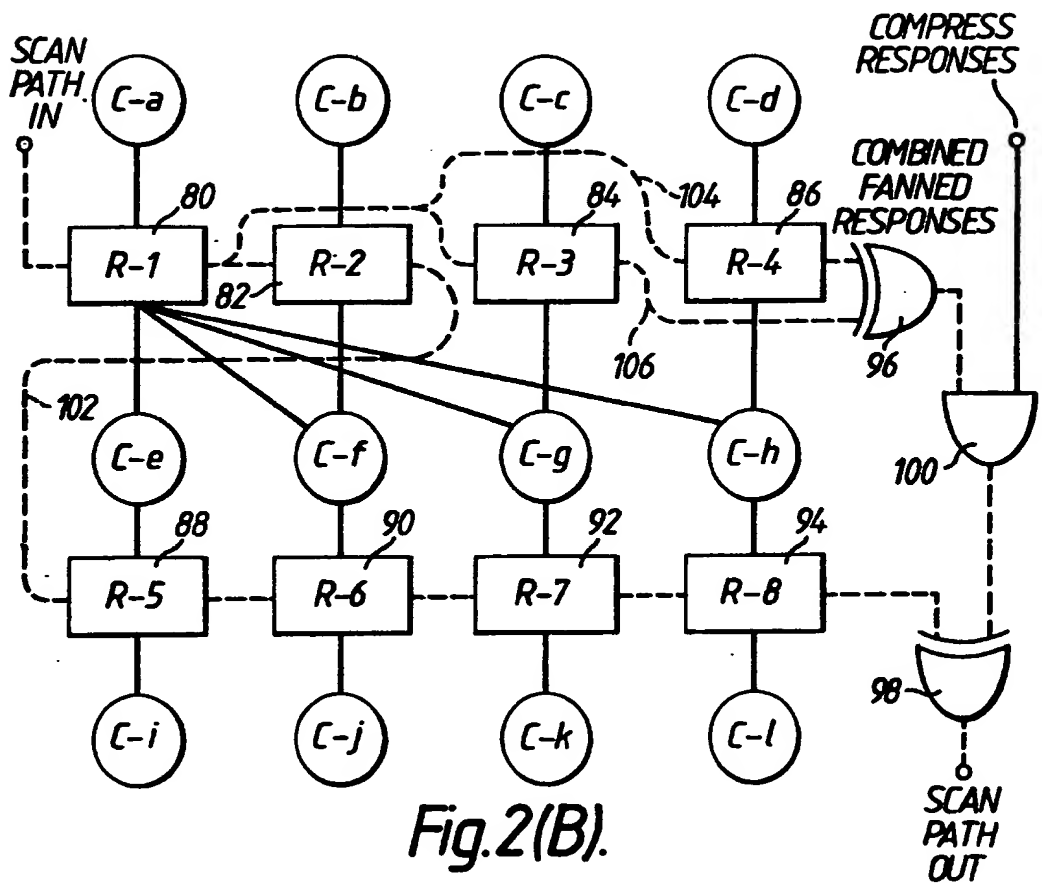

SCAN PATH IN
COMPRESS RESPONSES
COMBINED FANNED RESPONSES
C-a
C-b
C-c
C-d
80
82
84
104
86
R-1
R-2
R-3
R-4
106
96
102
100
C-e
C-f
C-g
C-h
88
90
92
94
R-5
R-6
R-7
R-8
98
C-i
C-j
C-k
C-l
SCAN PATH OUT

Fig.2(B).

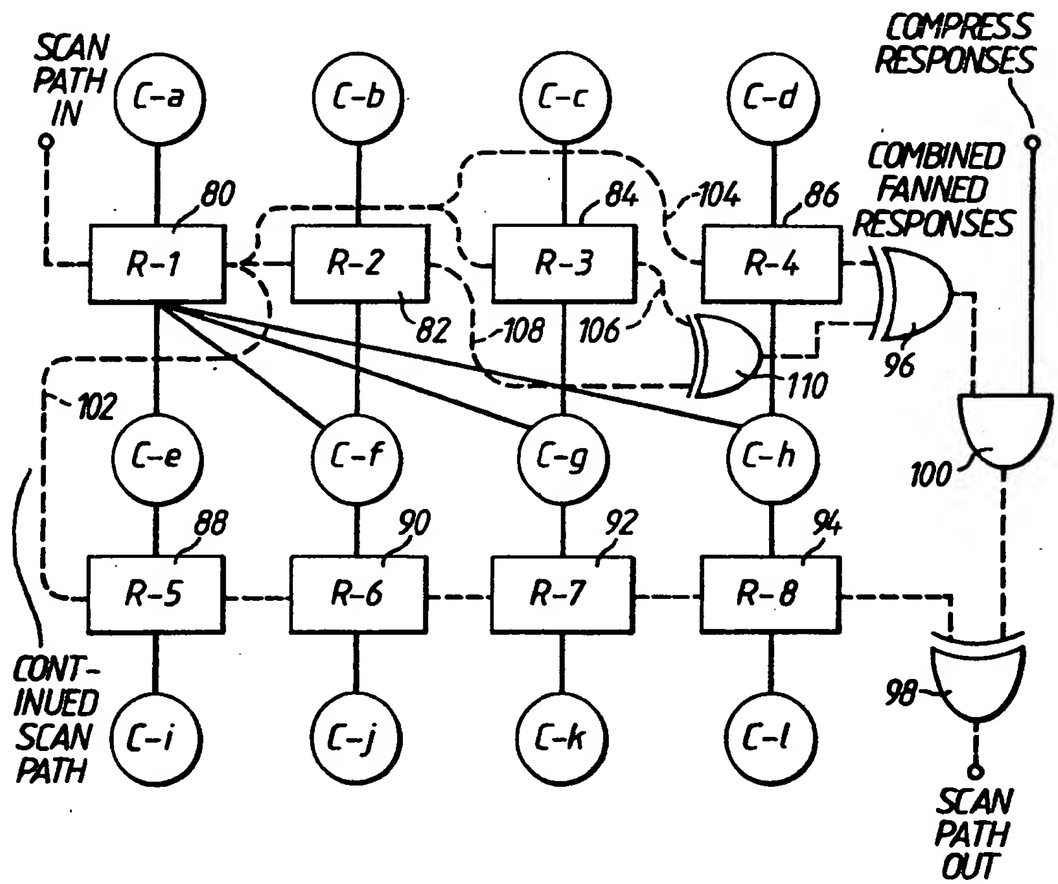

SCAN PATH IN
C-a
C-b
C-c
C-d
COMPRESS RESPONSES
COMBINED FANNED RESPONSES
80
84
104
86
R-1
R-2
R-3
R-4
82
108
106
96
110
102
100
C-e
C-f
C-g
C-h
88
90
92
94
R-5
R-6
R-7
R-8
98
CONT-INUED SCAN PATH
C-i
C-j
C-k
C-l
SCAN PATH OUT

Fig.2(C).

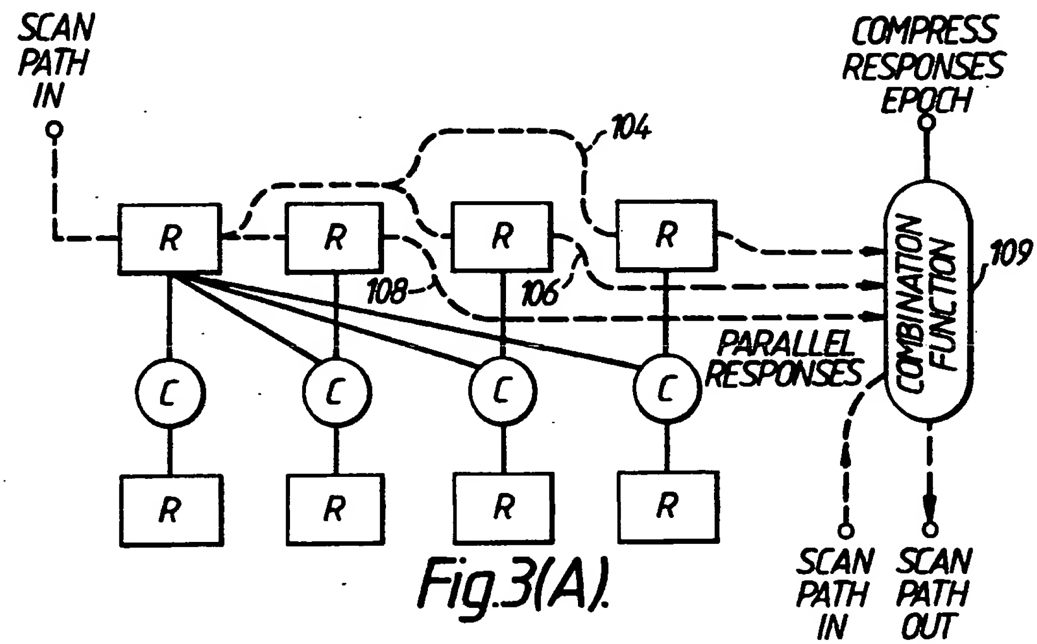


Fig.3(A).

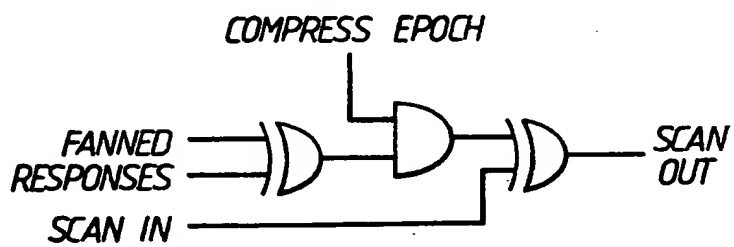


Fig.3(B).

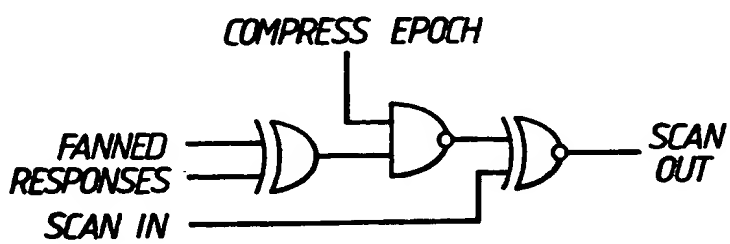


Fig.3(C).

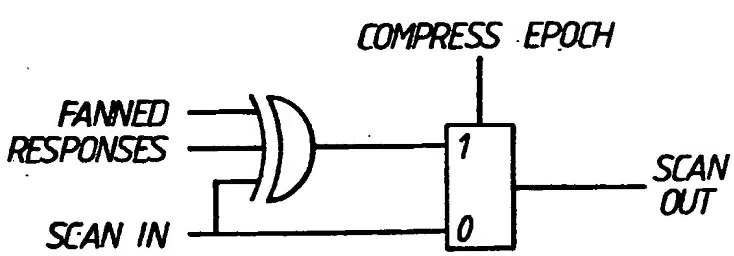


Fig.3(D).

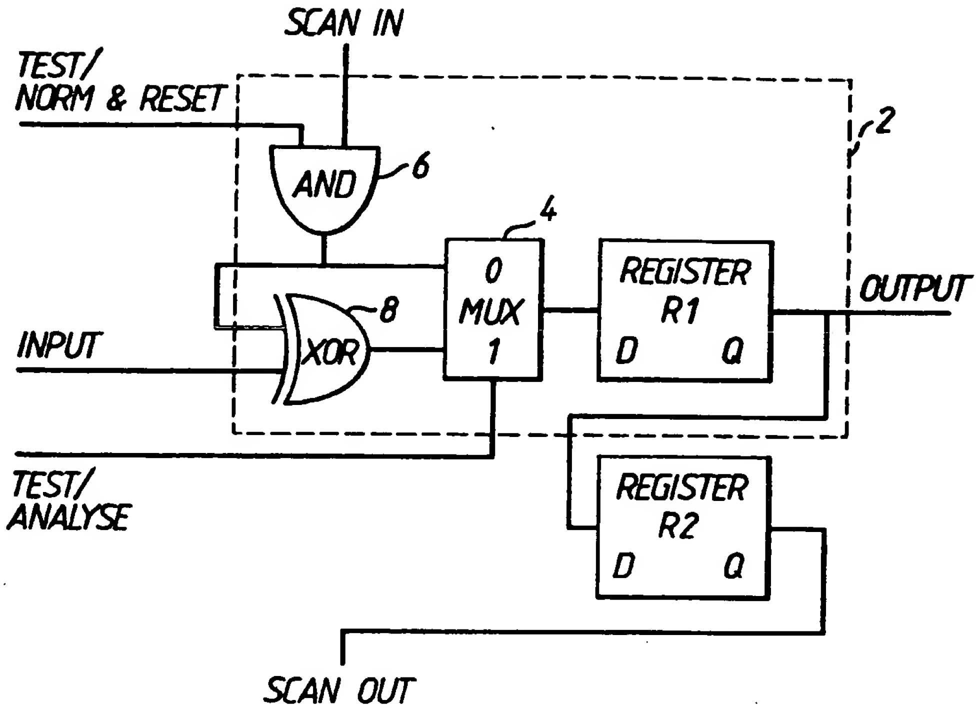

SCAN IN
TEST/
NORM & RESET
AND
6
4
2
0
MUX
1
REGISTER
R1
D
Q
OUTPUT
8
XOR
INPUT
TEST/
ANALYSE
REGISTER
R2
D
Q
SCAN OUT

Fig.4.

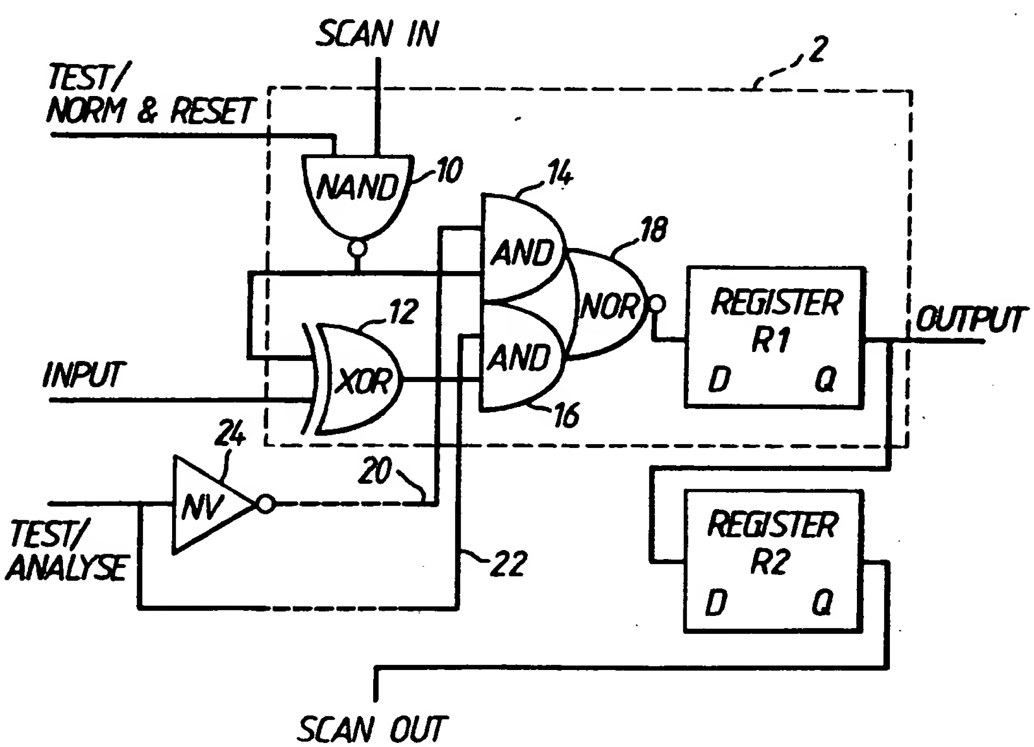

SCAN IN
2
TEST/
NORM & RESET
NAND
10
14
AND
18
NOR
REGISTER
R1
D
Q
OUTPUT
12
XOR
AND
16
INPUT
24
NV
20
TEST/
ANALYSE
22
REGISTER
R2
D
Q
SCAN OUT

Fig.5.

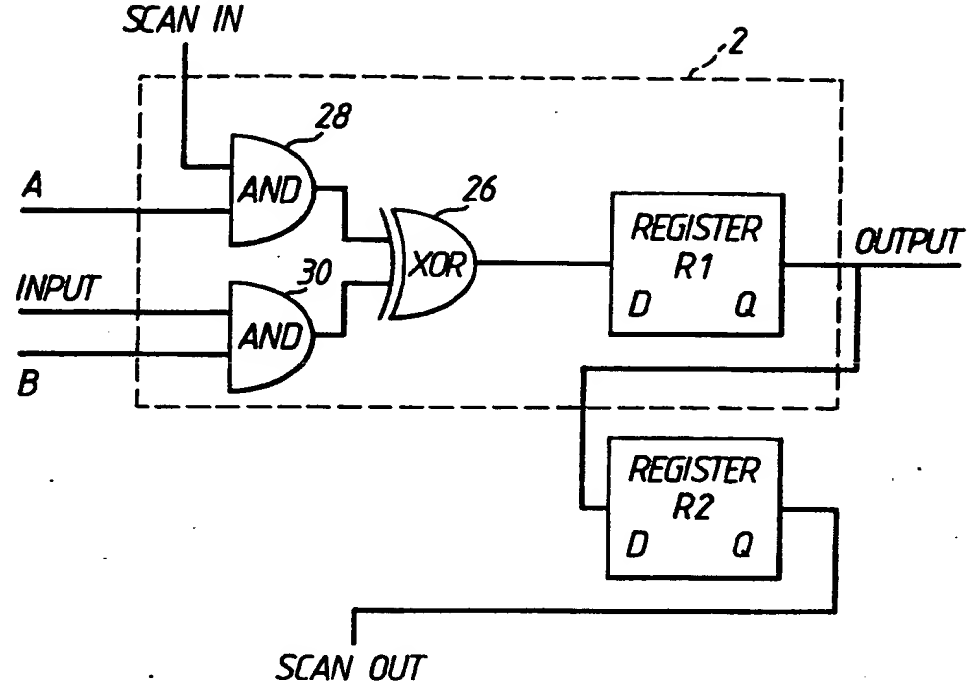

SCAN IN
2
28
A
AND
26
XOR
REGISTER
R1
D Q
OUTPUT
INPUT
30
AND
B
REGISTER
R2
D Q
SCAN OUT

Fig.6.

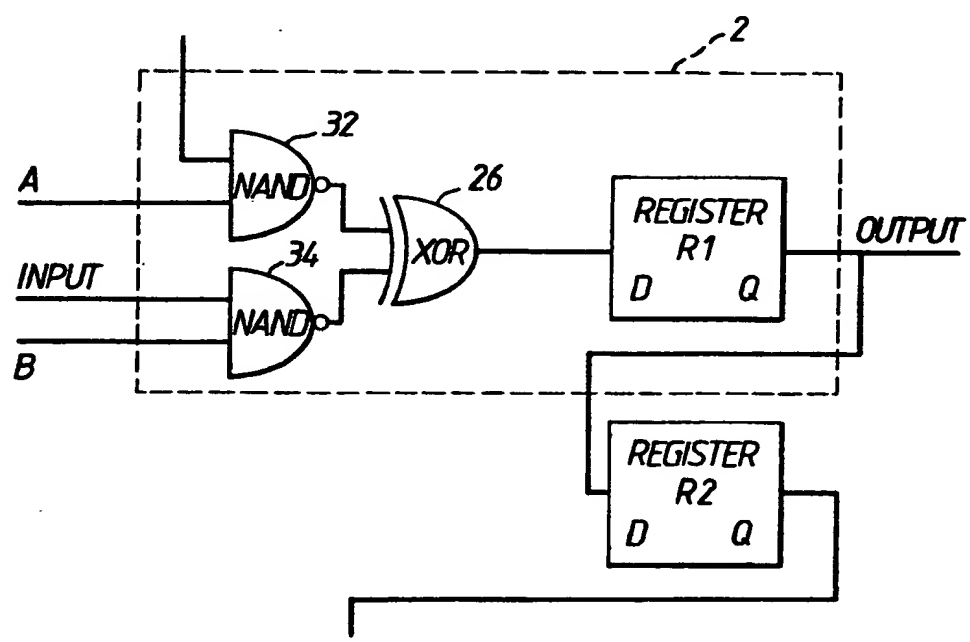

2
32
A
NAND
26
XOR
REGISTER
R1
D Q
OUTPUT
34
INPUT
NAND
B
REGISTER
R2
D Q

Fig.7.

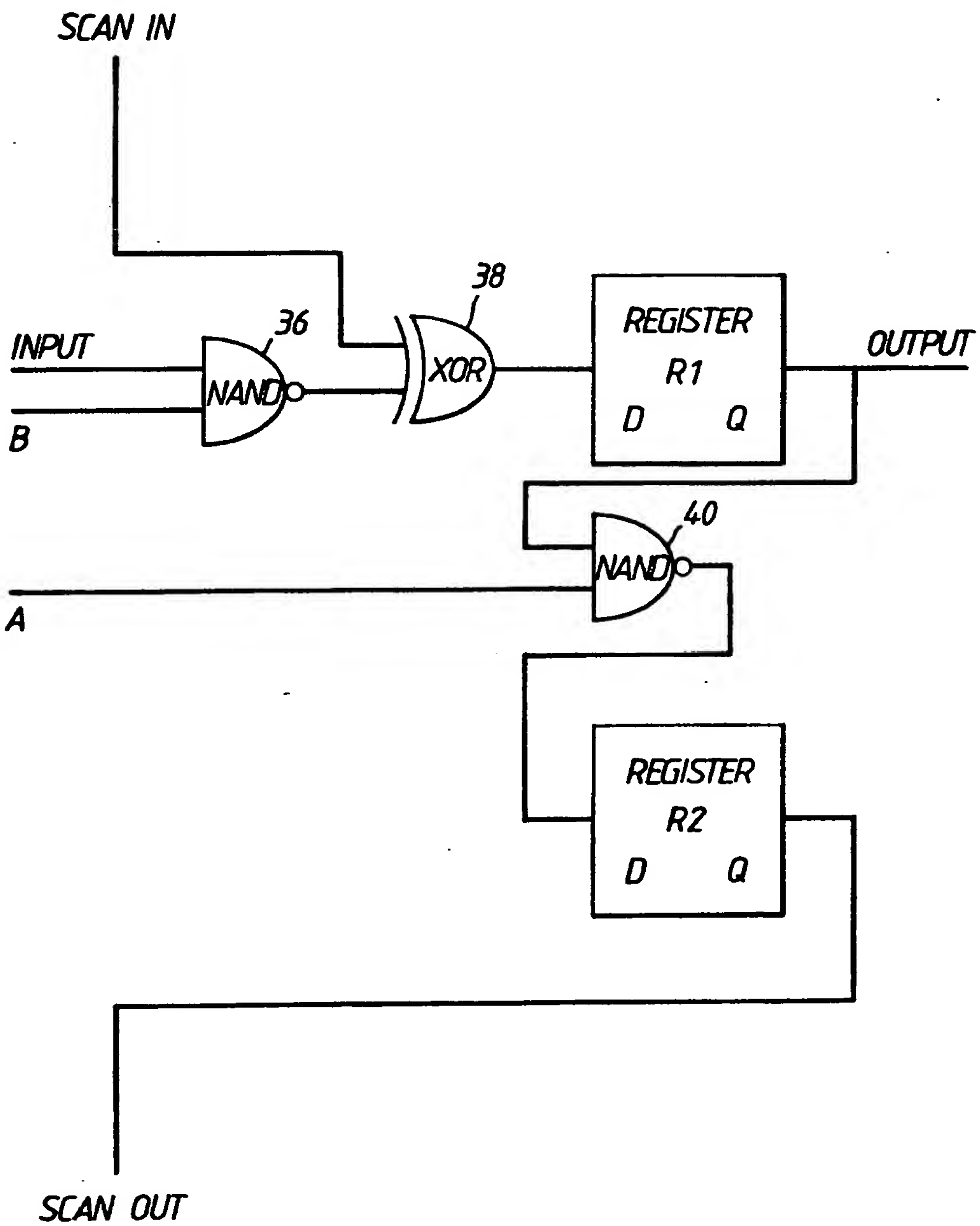

SCAN IN
38
36
INPUT
NAND
XOR
REGISTER
R1
D
Q
OUTPUT
B
40
NAND
A
REGISTER
R2
D
Q
SCAN OUT

Fig.8.

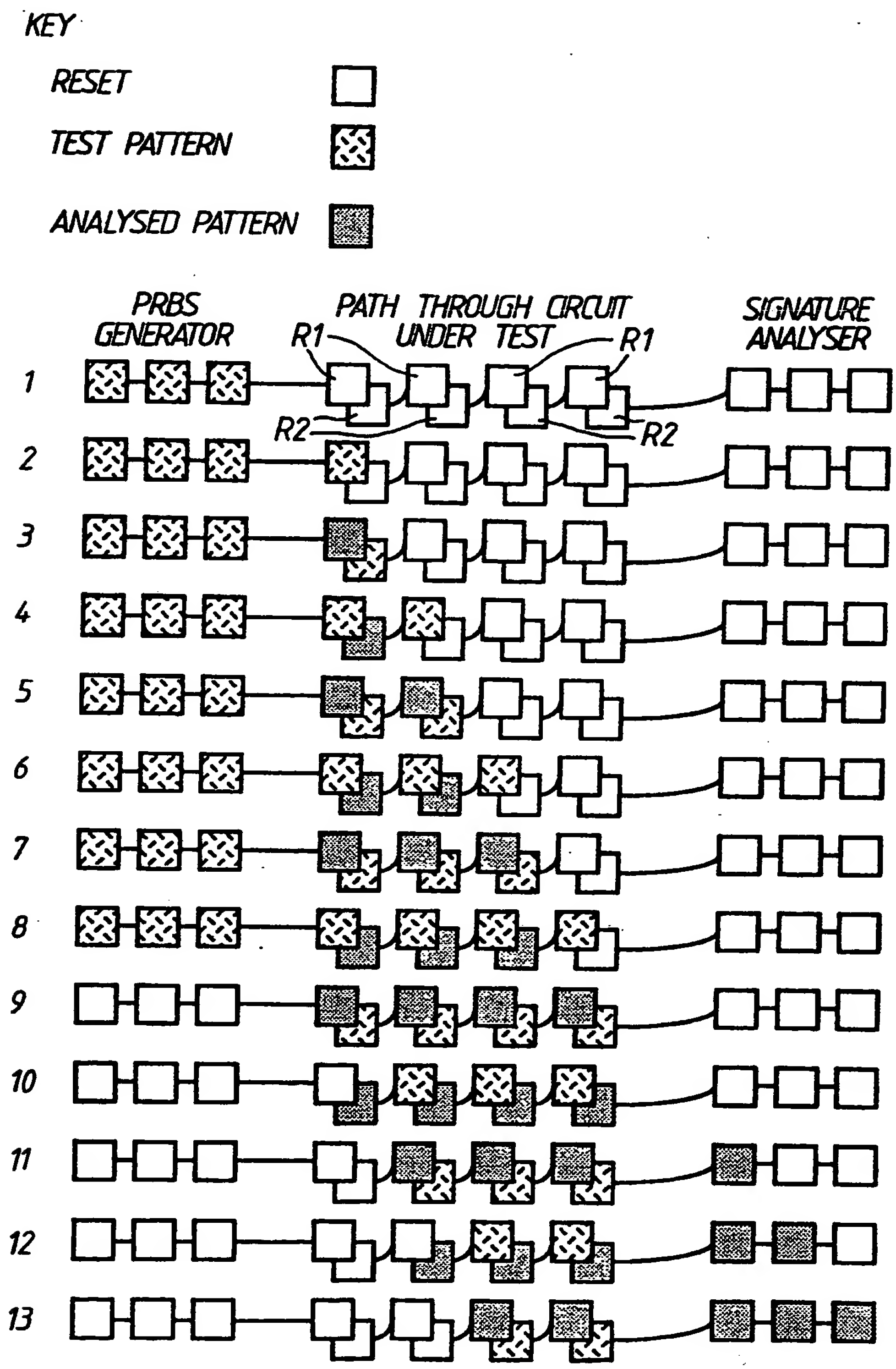
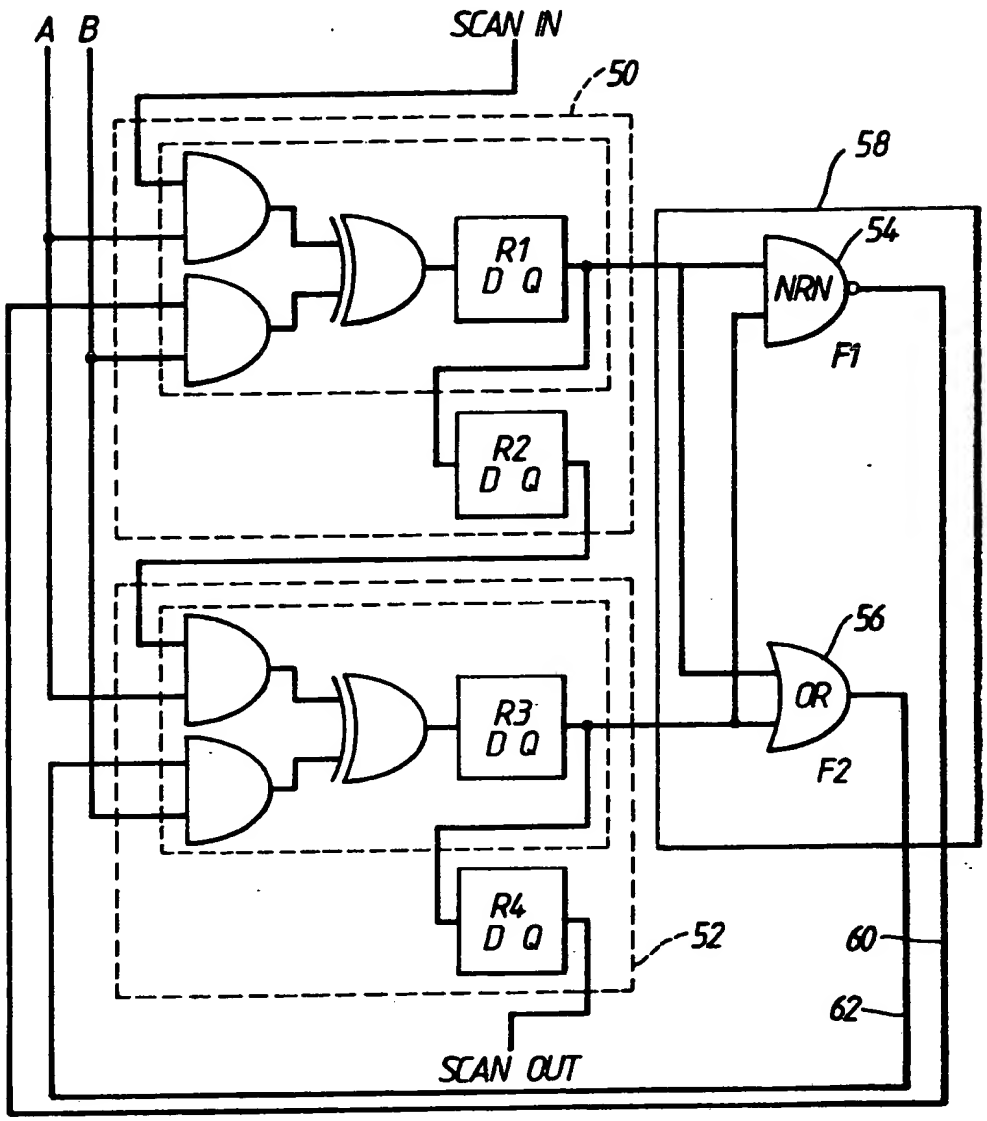

KEY
RESET
TEST PATTERN
ANALYSED PATTERN
PRBS GENERATOR
PATH THROUGH CIRCUIT UNDER TEST
SIGNATURE ANALYSER
R1
R1
R2
R2
1
2
3
4
5
6
7
8
9
10
11
12
13

Fig.9.



SCAN IN	A	B	R1	R2	R3	R4	F1	F2	SCAN OUT
0	0	0	0	x	0	x	1	0	x
0	0	0	0	0	0	0	1	0	0
1	1	1	1	0	0	0	1	1	0
0	1	0	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1	1	0
0	1	0	1	1	1	0	0	1	0
0	1	1	0	1	0	1	1	0	1
0	1	0	0	0	1	0	1	1	0
0	1	1	1	0	1	1	0	1	1
0	1	0	0	1	0	1	1	1	1
0	1	0	0	0	1	0	1	1	0
0	1	0	0	0	0	1	1	1	1

SCANNED SEQUENCE IN 00 110

STIMULATED F2 F1 01
11
10
11

SCANNED TEST RESULT OUT 00 011

Fig.10.

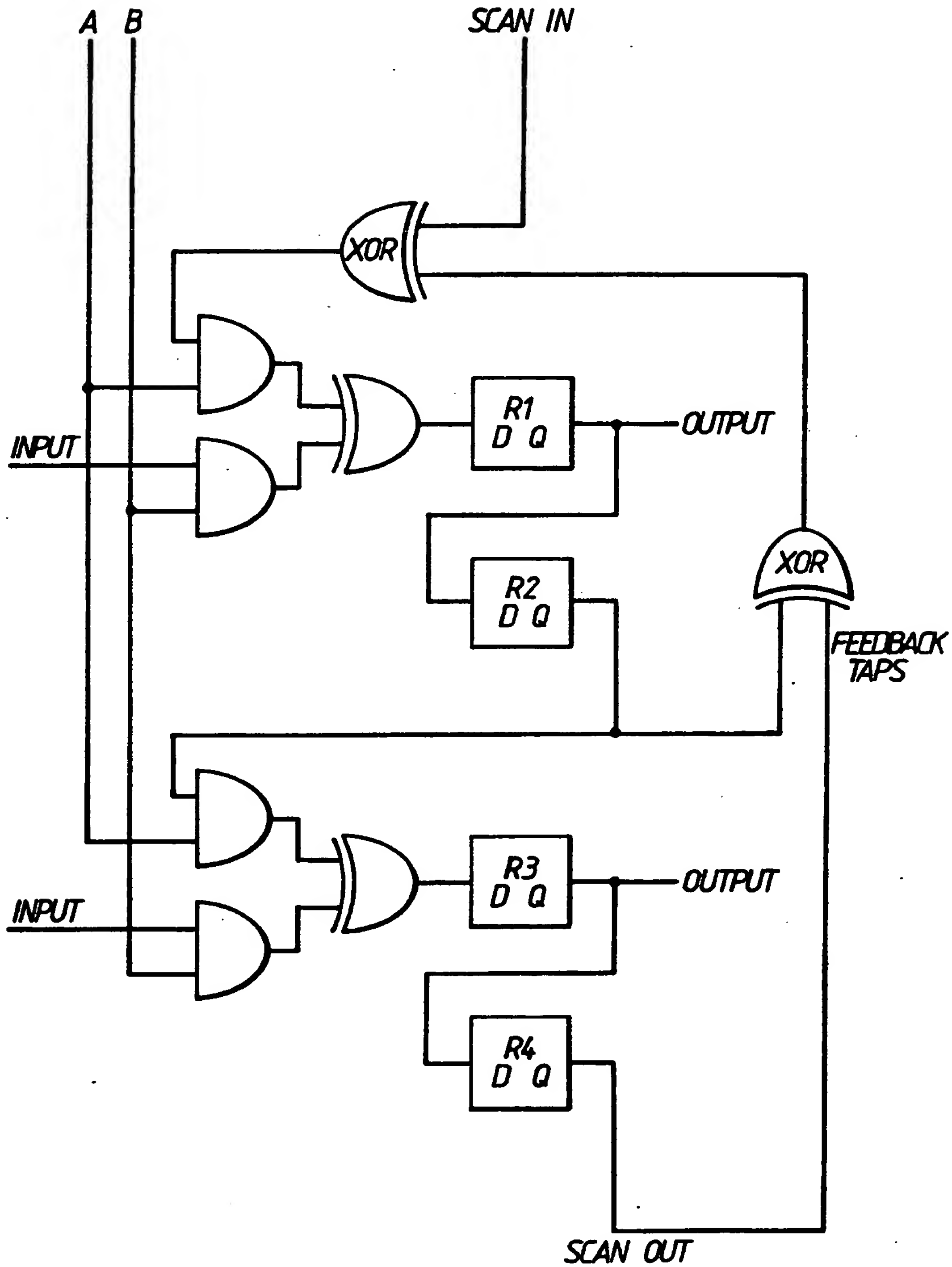
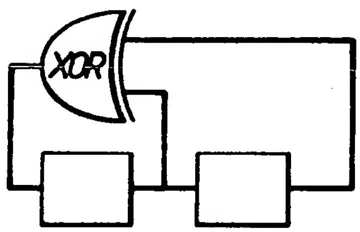
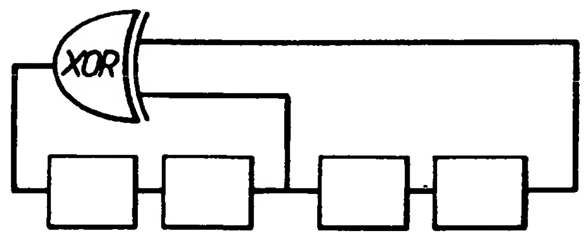

A
B
SCAN IN
XOR
INPUT
R1
D Q
OUTPUT
R2
D Q
XOR
FEEDBACK
TAPS
INPUT
R3
D Q
OUTPUT
R4
D Q
SCAN OUT

Fig.11.

NORMAL IMPLEMENTATION



INTERLEAVED TEST REGISTER IMPLEMENTATION



INITIALISATION		
	10	10 00
RUN		
		01 00
	11	10 10
		01 01
	01	00 10
		00 01
	10	10 00

NORMAL OUTPUT = 101

INTERLEAVED OUTPUT = 101 AND 000

Fig.12.

IMPROVEMENTS IN AND RELATING TO METHODS OF TESTING INTEGRATED CIRCUITS

The present invention relates to a method of testing integrated circuits and to an integrated circuit having a built-in self test design.

Digital circuits that operate synchronously are classed as circuit functions implemented by blocks of combinational logic which are buffered by flip-flops or latches forming registers.

Synchronous digital circuits may be tested by applying test patterns to the blocks of combinational logic and checking the output from these combinational blocks. If for a certain input width to a block of combinational logic all possible patterns are applied the combinational block will have been tested exhaustively.

An exhaustive set of input patterns for a given input width may be generated by a counter or more conveniently by a PRBS generator.

A means must be provided so that the test patterns may be applied to the combinational logic inputs and results checked from the combinational logic outputs. This generally involves configuring the registers on the inputs and the outputs of the combinational logic so that test patterns may be scanned through the circuit under test.

There are several known testing methods in which a digital circuits testability is enhanced by additional circuitry.

In the Level Sensitive Scan Design method the registers are configured into LSSD latches which may be selected to be normal registers or shift registers. The registers within the circuit are then combined into a single long scan path, down which data may be scanned when the registers are configured into shift mode. The

circuit is tested by shifting a test pattern down the scan path to stimulate the required combinational logic block. When a test pattern has been shifted to the correct position in the scan path, the circuit is clocked once in normal mode. This stimulates the inputs to the combinational logic and the resulting values are latched by the registers now on the outputs of the combinational logic. The captured data is then shifted down the scan path so that it may be checked.

The disadvantage in using this scheme is that only one test pattern may be applied at a time to the whole circuit, since the test pattern has been destroyed after the circuit under test has been clocked once in normal mode. A great deal of time is wasted in shifting test patterns down the scan path.

In some Built In Self Test schemes, the registers are Built In Logic Block Observation (BILBO) registers. BILBO registers may be configured to be parallel registers (Normal buffered mode), linear shift registers (Shift mode), parallel/shift data compression registers (Compression mode) and reset registers (Reset mode).

To test a block of combinational logic, the input registers are in Shift mode and may be configured as PRBS generators, whilst the output registers are in Compression mode and may be configured as parallel signature analysers. The combinational logic is then stimulated by a continuous stream of test patterns shifted through the input registers. The resulting data patterns are compressed with those latched in preceding cycles and continuously shifted out to be analysed.

This scheme has numerous complications when testing many interlinked logic blocks. The fundamental problem relates to the fact that when a register is providing test patterns it may not compress any results, since in doing this the test pattern would be lost.

This problem causes a number of technical complications such as how a circuit containing a chain of logic blocks is be tested.

A solution to this complication is to use test phases, so that in one phase a register may be providing test patterns, whilst in another phase the register is compressing data resulting from other logic blocks under test. This principle is illustrated in Figures 1A and 1B. Often several test phases are required to ensure that all logic blocks have been tested. An added complication is that the sequence of input scan registers to test blocks of combinational logic in one test phase is not that required for another test phase, requiring reconfiguration of the scan path through the circuit. This reconfiguration entails the use of many serial multiplexers, whilst the selection of test phases requires the routing of many test phase control busses and their associated decoders to drive the BILBO registers. The addition of decoders to drive the BILBO registers introduces another problem, since it is very awkward to verify that the BILBO register can return to normal operation (due to failure of the decoder) an additional test line is required to the register. One solution to this problem is the Structured Test Register described in European Patent Application No. 85308852.4 the contents of which are incorporated herein by reference.

A further complication arises as to how a circuit containing a logic block in which the outputs are fed directly back to the inputs

may be tested Figure 1(C). The solution to this complication is illustrated in Figure 1(D) and is described fully in European Patent Application No. 85308521.5 the contents of which are incorporated herein by reference. The solution is to split the feedback path around the block of combinational logic using a multiplexer (mux) and an additional BILBO register (Rt) in another test phase, so that by suitable switching, one register may generate test patterns whilst the other compresses the results.

Both of the above solutions to the complications arising from the BILBO scheme may be complex to solve for a real circuit and may require a great deal of circuit area to implement.

The LSSD scan path scheme is easy to overlay on the circuit under test and fairly compact, however the scheme takes a long time to test, and if non-exhaustive testing is employed a great deal of effort is required to generate the test patterns.

The Built in Self Test schemes such as BILBO quickly test the circuit, however when blocks are interconnected the scheme is not compact and very complicated to overlay.

The basic problem with previous schemes is that they may only capture test results when not generating test patterns, since the test pattern held by a register is overwritten when a test result is captured.

The above difficulties are particularly a problem in the self testing of a circuit arrangement in which a number of combinational logic blocks are driven by a common input register and each combinational logic block is also driven by its own input register. With previous testing methods the scan path is routed through all of

the registers which requires a large test pattern and difficulties are encountered in conserving previously obtained analysed data.

According to the present invention there is provided an integrated circuit having a built-in self test design, the integrated circuit comprises a plurality of combinational logic blocks and a plurality of test registers, the test registers being responsive to signals for selectively controlling their functional modes and being coupled together to define a plurality of interleaved test registers, each interleaved test register comprising at least two registers to provide at least a two stage delay whereby in operation one of the delay stages holds test patterns whilst the other delay stage holds compressed test results, the arrangement being such that the combinational logic blocks are arranged to be driven by a common input interleaved test register and each of the combinational logic blocks is also arranged to be driven by a respective input interleaved test register, the outputs of each of the combinational logic blocks being coupled to respective output interleaved test registers, a scan path being routed through the common interleaved test register and diverged into a plurality of scan paths through the input interleaved test registers, the scan paths reconverging at a logic function comprising an Exclusive - OR or an Exclusive - NOR function for modulo-2 addition on the incoming streams of data from the scan paths or selecting one of the streams of data on a single scan path whereby in operation information is provided which is representative of all of the analysed information including any analysed information originally presented to the common interleaved

test register or the test pattern information originally presented to the common interleaved test register, conserved for later re-use.

The method of testing an integrated circuit having a built-in self test design which employs interleaved test registers comprises the step of multiplexing the test generation and test result compression by employing a time division multiplexing technique whereby the compressed test results are stored in intermediate memory elements interleaved between memory elements that store the original test patterns that stimulated those test results.

The interleaved test register can concurrently generate test patterns and compress test results from a logic block by multiplexing the test generation and test result compression in time, rather than completing one before starting another. During test mode, the circuit timing may be divided into two epochs, test and compress. This test method is hereinafter referred to as the Interleaved Test Method, due to this time division multiplexing.

In order to realise this concept, a register must be provided that can store a test pattern when compressing in a test result, and store the compressed test result when outputting a test pattern.

The interleaved test register in a preferred embodiment operates in the following modes:

Normal mode, in which the register buffers parallel information;

Shift mode, in which register linearly shifts data through a serial scan path;

Compression mode, in which the register compresses the parallel and shifted inputs, and;

Reset mode, in which the register may be set or reset.

However its timing behaviour is very different from previous test registers, which allows the register to be used in the Interleaved Test Method.

In normal operation, the register acts as a unit delay between input and output signals. However during scan or compression mode, the interleaved test register acts as a two stage delay between input and scan output. By utilising this two stage delay during test, one delay stage can be holding test patterns whilst the second delay stage holds compressed test results.

In one embodiment of the integrated circuit the first register in each group is arranged for receiving data from a scan path input and/or a data input, and for providing output data to a combinatorial logic block and for the second register, the second register being arranged for providing output data to either a scan path output of the interleaved test register or, if there are more than two registers in the group, to the combinatorial logic block and to a further register.

In another embodiment the interleaved test register (ITR) comprises two registers and the ITR is arranged to be operative in at least four basic modes including:-

A Normal Mode in which the ITR latches input data on the input, acting as a buffer or register with one unit of delay;

A Scan Mode in which the ITR latches scan data on the scan path, presenting two units of delay to the scan path through the ITR, and whereby the combinatorial logic block to be tested is stimulated

by the data held by the input register that is in use during Normal Mode;

A Compress Mode in which the ITR latches a test result given by a modulo-2 addition (XOR or XNOR) of the input data on the ITR input and the scan path data on the scan path through the ITR, two units of delay being presented to the scan path through the ITR; and

A Reset Mode in which the two registers within the ITR are set or reset, depending on implementation.

The present invention will be described further, by way of example, with reference to the accompanying drawings in which:-

Figures 1(A), 1(B), 1(C) and 1(D) illustrate in block form examples of known built-in self test circuit arrangements,

Figures 2(A) and 2(B) illustrate in block diagram form circuits for testing logic blocks with a shared input, Figure 2(B) being an embodiment according to the present invention,

Figure 2(C) illustrates in block form another embodiment of the present invention,

Figure 3(A) illustrates in block schematic form a further embodiment of the present invention; and

Figures 3(B), 3(C) and 3(D) are typical implementations in accordance with embodiments of the invention of the combination function illustrated in Figure 3(A),

Figures 4 to 8 illustrate in block form different embodiments of interleaved test register elements according to the present invention,

Figure 9 illustrates in simplified diagrammatic form how an interleaved test signal is transmitted through circuitry incorporating interleaved test registers like those of Figures 4 to 8.

Figure 10 illustrates in block form a manner in which interleaved test register elements of Figure 6 can be arranged to test a combinational logic circuit,

Figure 11 illustrates in block form a PRBS generator and a LFSR (linear feedback shift register) constructed from ITR elements and,

Figure 12 illustrates the PRBS sequence of the PRBS generator of Figure 11.

There are frequent circuit configurations where a collection of combinational logic blocks are driven by a common input register and each combinational block is also driven by its own input register. This may be tested by routing the scan path through all the registers R involved, but this may require a large test pattern to test exhaustively. Such an arrangement is illustrated in Figure 2(A). In which combinational logic blocks c-e, c-f, c-g and c-h are all driven by a common input register R-1 the input of which is itself connected to the output of a combinational logic block c-a. Register blocks R-2, R-3 and R-4 drive respective combinational logic blocks c-f, c-g and c-h and inputs of register blocks R-2, R-3 and R-4 are connected to respective outputs of combinational logic blocks c-b, c-c and c-d. The outputs of combinational logic blocks c-e, c-f, c-g and c-h are fed to respective register blocks R-5, R-6, R-7 and R-8 the outputs of which are connected to respective combinational blocks c-i, c-j, c-k and c-l.

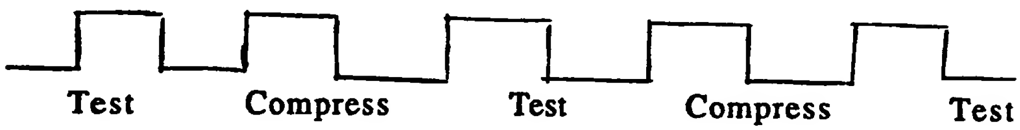
An alternative and an embodiment of the present invention is illustrated in Figure 2(B). The modifications to the circuit paths of Figure 2(A) are shown by the dotted lines in Figure 2(B). In Figure 2(B) the scan path is routed through a common input interleaved test register 80 and then allowed to diverge through individual input

interleaved test registers 82, 84, 86 and output interleaved test registers 88, 90, 92 and 94. The scan paths then reconverge at an XOR or XNOR function that performs modulo-2 addition on the incoming streams to conserve the analysed information. In Figure 2(B) two XOR gates 96, 98 and an AND gate 100 are provided. All the diverging scan paths but one (the longest path 102) are masked during the test pattern epoch when converging by the absence of an enabling pulse on the input of the AND gate 100. The original test pattern information is preserved along the continued scan path 102. Enabling pulses to the AND gate 100 are timed to ensure information is provided which is representative of the analysed information from scan paths 104 and 106.

Figure 2(C) illustrates another embodiment of the present invention. The modifications over the embodiment of Figure 2(B) are the insertion of a further XOR gate 110 in the scan path 106, a scan path 108 between the output of the interleaved test Register 82 and an input of XOR gate 110, and the continued scan path 102 now leading directly from the output of the common interleaved test register 80 to the input of the interleaved test register 88. The modifications to the circuit paths of Figure 2(A) are shown by the dotted lines in Figure 2(C).

A further more general embodiment of the present invention is illustrated in block schematic form in Figure 3(A), the modifications to the circuit paths of Figure 2(A) being shown by the dotted lines in Figure 3(A). The logic function for modulo-2 addition is illustrated generally by a combination function block 109. Examples of typical logic function implementations of the combination function 109

illustrated in Figure 3(A) are shown in Figures 3(B), 3(C) and 3(D). The test patterns are applied in two epochs - a test pattern application epoch and a response compaction epoch such as:-



The Interleaved Test Register may be devised by creating a test register with two delay elements. The additional delay element, such as a buffer or a flip flop, is joined to the scan output of the register. Since this additional delay element is only utilised during self test, it may be implemented as a dynamic memory element, greatly saving circuit area. Examples of Interleaved Test Register implementations are illustrated in Figures 4 to 8.

An embodiment of an Interleaved Test Register is illustrated in Figure 4. The components within a BILBO block 2, defined within the dotted line, and their mode of operation are similar to those found in known BILBO self-test circuitry design. The design of the BILBO block 2 is based on the use of a multiplexer 4 coupled between the outputs of a pair of logic gates 6, 8 and the input of a Register R1. The logic gates 6 and 8 are AND and exclusive OR gates respectively. The Register R1 acts as a first delay element and the output of the Register R1 will in practice be connected to the input of a combinational logic circuit (not shown) to be tested. A major feature of the embodiment of Figure 4 is the provision of a second delay element in the form of an additional Register R2 connected to the output of the Register R1. The Registers R1 and R2 together provide

during a test operation a two stage delay, one of the delay stages holding test patterns whilst the other delay stage holds compressed test results, the output of the additional Register R2 being the scan out output.

A further embodiment of an Interleaved Test Register is illustrated in Figure 5 in which the logic gates 6, 8 of Figure 4 are replaced by logic gates 10, 12 in the form of a NAND gate and an Exclusive OR gate respectively. The multiplexer is shown as an arrangement of two AND gates 14, 16 the outputs of each of which are connected to a respective input of a NOR gate 18. The output of the NOR gate 18 is connected to the input of the Register R1. The test analyse signal line is split into two lines 20, 22 connected respectively to inputs of the AND gates 14, 16. The line 20 incorporates an inverter 24.

Figures 6 and 7 illustrate two further embodiments of an Interleaved Test Register. In each of the BILBO blocks 2 the multiplexer of Figures 4 and 5 has been replaced by an Exclusive OR gate 26 the inputs of which are driven via either a pair of AND gates 28, 30 (Figure 6) or a pair of NAND gates 32, 34 (Figure 7).

A further embodiment of an Interleaved Test Register is illustrated in Figure 8 in which the BILBO block 2 of Figures 4 to 6 is replaced by a pair of logic gates 36, 38, the logic gate 36 being a NAND gate the output of which is connected to one of the inputs of an Exclusive OR gate 38 the other input of which is connected to the Scan In input. The Register configuration in Figure 8 has its scan path interrupted between the Register R1, R2 by a NAND gate 40.

To use the Interleaved Test Register within the Interleaved Test Methodology, all the registers on the inputs of logic blocks would be configured to form a scan path, or collection of scan paths. If the circuit is to be tested exhaustively by a set of input patterns, the input registers should be arranged so that all common inputs to logic blocks are arranged continuously along the scan path, although other methods may be used to ensure that every set of inputs to combinational logic blocks receive an exhaustive set of test patterns. A block may be tested exhaustively by a linear test pattern generator such as a PRBS generator of length equal to the maximum block input width. All smaller input widths to blocks will be automatically covered. The sequence of operations during test are given in Figure 9. The scan path through the circuit to be tested is illustrated diagrammatically by four pairs of Interleaved Registers R1, R2 arranged in a chain arrangement. Test signals are fed as alternate signals from a PRBS Generator to the first Register R1 in the chain. The outputs of the Registers R1 are connected to logic circuitry associated with one or more Combinational Logic Blocks (not shown) to be tested. The Register R2 in each pair has its input connected directly or indirectly via a logic gate, to the output of a respective one of the Registers R1; and the scan outputs of the first three Registers R2 in the chain are connected to the inputs of respective Registers R1. The fourth Register R2 at the end of the chains has its output connected to a Signature Analyser. An example of a circuit under test is given in Figure 10.

Figure 10 illustrates in block form a circuit having two interleaved test register elements 50, 52 each of which has a

construction like that shown in Figure 6. The output of the elements 50,52 is connected to logic elements 54, 56 within a combinational logic circuit 58 under test. Feedback lines 60, 62 couple the output of the logic elements 54, 56 back to an input of the respective element 50,52. In operation the test pattern remains unchanged but the test results, that is the compressed results, change as they are shifted between the interleaved test registers. A typical logic sequence diagram is shown in Figure 10 to illustrate the stimulated outputs F1, F2 from logic elements 54,56 from a scanned in sequence.

The ITR is configured by 2 global signals to select Normal, Scan, Compress and Reset modes.

The interleaved test method can be easily overlayed on circuits, since in its simplest form only one scan path is involved, reconfiguration of this scan path and additional test phases are not necessary for combinational logic. Since the test registers both output test patterns and compress test results, complex interconnections of logic blocks and local feedback may be easily tested.

The test patterns may be provided by a PRBS generator. This generator should deliver a new pattern every two clock cycles. This may be accomplished by a PRBS generator with hold on its delay elements, or the registers at the head of the scan path may be incorporated within a PRBS generator if the data inputs to the ITR were held low. It should be noted that a PRBS generator constructed from ITR elements is capable of generating two independant PRBS sequences.

The test results shifted down the scan path may be analysed by a signature analyser. This may be incorporated within the registers at the tail of the scan path. It should be noted that a signature analyser constructed from ITR elements is capable of serially compressing two input sequences into two independant signatures. Alternatively a sequence may be analysed as an independant PRBS sequence is concurrently produced. An example of a PRBS generator is implemented in Figure 11. It is PRBS sequence is given in Figure 12.

Although the present invention has been described above with respect to particular embodiments, it should be understood that modifications may be effected within the scope of the invention.

CLAIMS:

1. An integrated circuit having a built-in self test design, the integrated circuit comprises a plurality of combinational logic blocks and a plurality of test registers, the test registers being responsive to signals for selectively controlling their functional modes and being coupled together to define a plurality of interleaved test registers, each interleaved test register comprising at least two registers to provide at least a two stage delay whereby in operation one of the delay stages holds test patterns whilst the other delay stage holds compressed test results, the arrangement being such that the combinational logic blocks are arranged to be driven by a common input interleaved test register and each of the combinational logic blocks is also arranged to be driven by a respective input interleaved test register, the outputs of each of the combinational logic blocks being coupled to respective output interleaved test registers, a scan path being routed through the common interleaved test register and diverged into a plurality of scan paths through the input interleaved test registers, the scan paths reconverging at a logic function comprising an Exclusive - OR or an Exclusive - NOR function for modulo-2 addition on the incoming streams of data from the scan paths or selecting one of the streams of data on a single scan path whereby in operation information is provided which is representative of all of the analysed information including any analysed information originally presented to the common interleaved test register or the test pattern information originally presented to the common interleaved test register, conserved for later re-use..

2. An integrated circuit having a built-in self test design, as claimed in claim 1 wherein means are provided for multiplexing the test generation and test result compression by employing a time division multiplexing technique whereby the compressed test results are stored in intermediate memory elements interleaved between memory elements that store the original test patterns that stimulated those test results.

3. An integrated circuit having a built-in self test design as claimed in Claim 1 or Claim 2, wherein the test registers are coupled together in groups, each group comprising at least two registers and defining together with other logic elements an interleaved test register, the registers in each group providing at least a two stage delay whereby in operation one of the delay stages holds test patterns whilst the other delay stage holds compressed test results.

4. An integrated circuit as claimed in claim 3 wherein the first register in each group is arranged for receiving data from a scan path input and/or a data input, and for providing output data to a combinatorial logic block and for the second register, the second register being arranged for providing output data to either a scan path output of the interleaved test register or, if there are more than two registers in the group, to the combinatorial logic block and to a further register.

5. An integrated circuit as claimed in claim 3 or 4 wherein the interleaved test register (ITR) comprises two registers and the ITR is arranged to be operative in at east four basic modes including:-

A Normal Mode in which the ITR latches input data on the input, acting as a buffer or register with one unit of delay;

A Scan Mode in which the ITR latches scan data on the scan path, presenting two units of delay to the scan path through the ITR, and whereby the combinatorial logic block to be tested is stimulated by the data held by the input register that is in use during Normal Mode;

A Compress Mode in which the ITR latches a test result given by a modulo-2 addition (XOR or XNOR) of the input data on the ITR input and the scan path data on the scan path through the ITR, two units of delay being presented to the scan path through the ITR; and

A Reset Mode in which the two registers within the ITR are set or reset, depending on implementation.

6. An integrated circuit as claimed in any one of claims 3 to 5 wherein a number of combinational logic blocks are arranged to be driven by a common input register and each combinatorial logic block is also arranged to be driven by its own input register, the scan path being routed through the common input register then diverged through the individual input registers, the scan paths then reconverging at an XOR or XNOR function for performing modulo-2 addition on the incoming streams of data to conserve the analysed information during a self test operation or the test pattern information originally presented to the common interleaved test register, for later re-use.

7. A method of testing an integrated circuit having a built-in self test design, the method being substantially as hereinbefore described.

8. An integrated circuit having a built-in self test design, the integrated circuit having substantially as hereinbefore described

with reference to each of the embodiments illustrated in the figures of the accompanying drawings.

Published 1989 at The Patent Office, State House, 66/71 High Holborn, London WC1R 4TP. Further copies maybe obtained from The Patent Office. Sales Branch, St Mary Cray, Orpington, Kent BR5 3RD. Printed by Multiplex techniques ltd, St Mary Cray, Kent, Con. 1/87

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